AU-B0001: AMBA AHB/APB Bus Bridge Core

The AMBA AHB/APB Bus Bridge is a bridge between an AMBA AHB Bus and an AMBA APB Bus. It includes the slave select line decoder for the AMBA APB Bus. Sixteen AMBA APB Bus slaves are supported. The AMBA AHB/APB Bus Bridge is available as a synthesizable Verilog model from Aurora VLSI, Inc. Contact CustomerService@auroravlsi.com.

The AMBA AHB/APB Bus Bridge is an AMBA AHB Bus slave. It accepts all AMBA AHB Bus transactions that target it. It examines the AMBA address of these transactions and if the address falls within an AMBA APB Bus slave address space, it asserts that slave's select signal and drives the transaction onto the AMBA APB Bus to the selected slave. If the transaction is a read, the AMBA AHB/APB Bus Bridge captures the read data from the AMBA APB Bus and drives it onto the AMBA AHB Bus. To complete the AMBA transaction, the AMBA AHB/APB Bus Bridge drives the OKAY AMBA response onto the AMBA AHB Bus.

The AMBA AHB/APB Bus Bridge supports all AMBA AHB transaction types and burst types. The AMBA APB Bus is a 32 bit bus. Therefore, AMBA AHB data sizes of one, two, and four bytes are supported by the AMBA AHB/APB Bus Bridge.

The AMBA AHB/APB Bus Bridge contains sixteen programmable address registers- one address register per AMBA APB Bus slave. These registers hold the base address and size of each AMBA APB Bus slave's address space.

The AMBA AHB Bus clock and AMBA APB Bus clock may be the same clock or separate asynchronous clocks.

AMBA AHB/APB Bus Bridge features are summarized:

- AMBA AHB Bus to APB Bus bridge function
- AMBA APB Bus decoder function
- 16 AMBA APB Bus slaves
- Supports all AMBA AHB Bus transaction types
- Supports all AMBA AHB Bus burst types
- Supports AMBA AHB data sizes of 1, 2, and 4 bytes
- 16 slave address registers- one register per slave
  - base address of the slave's address space
  - size of the slave's address space
- Synchronous or asynchronous AMBA AHB bus clock and AMBA APB bus clock

The core is delivered as a synthesizeable RTL Verilog model. Deliverables include:

- RTL Verilog source code model of the core
- Verilog testbench and test cases
- Synthesis scripts examples
- Complete detailed documentation and training class notes