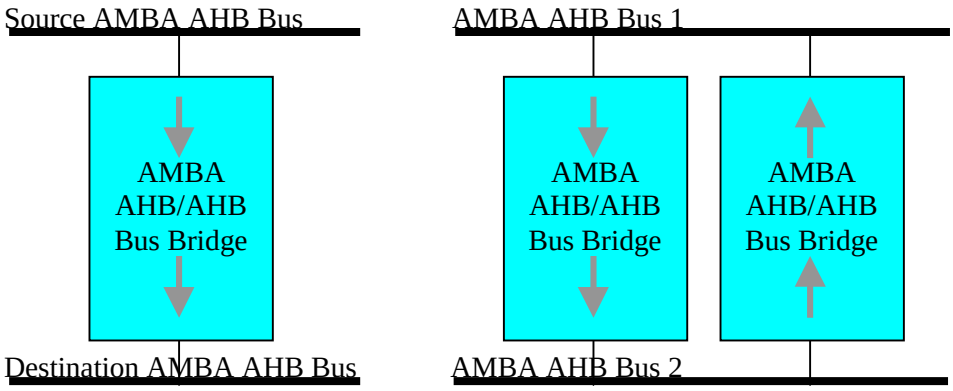
AU-B0002: AMBA AHB/AHB Bus Bridge Core

The AMBA AHB/AHB Bus Bridge is a unidirectional bridge between two AMBA AHB buses. It drives a transaction from a source AMBA AHB bus to a destination AMBA AHB bus. A full bidirectional bridge is implemented using two AMBA AHB/AHB Bus Bridges in parallel, with each pointing in the opposite direction of the other. The AMBA AHB/AHB Bus Bridge is available as a synthesizable Verilog model from Aurora VLSI, Inc. Contact CustomerService@auroravlsi.com.



Unidirectional AMBA AHB Bridge Full Bidirectional AMBA AHB Bridge

The AMBA AHB/AHB Bus Bridge supports up to 64 address spaces on the destination AMBA bus. These may be the address spaces of AMBA slaves on the destination bus. Alternatively, they may be address spaces "behind" another bridge on the destination AMBA bus.

The AMBA AHB/AHB Bus Bridge supports all AMBA AHB data sizes, transaction types, and burst types. Additionally, both the source and destination AMBA buses can be independently configured to be either 32 bit or 64 bit AMBA buses. The AMBA AHB/AHB Bus Bridge is optimized to make efficient use of the destination AMBA bus. Write data from the source AMBA bus is packed into transactions of the largest possible data size on the destination AMBA bus. Read transactions on the destination AMBA bus also use the largest possible data size. The read data from the destination bus is unpacked according to the source AMBA bus transaction data size, when returning it on the source AMBA bus. On reads, depending to the burst type, the AMBA AHB/AHB Bus Bridge prefetches data on the destination AMBA bus so that the peak data rate can be maintained during bursts

The source AMBA bus clock and destination AMBA bus clock may be the same clock or separate asynchronous clocks.

AMBA AHB/AHB Bus Bridge features are summarized:

- Unidirectional source AMBA bus to destination AMBA bus bridge function
- Bidirectional bridge implemented with two instantiations
- 32 bit or 64 bit source AMBA bus- user configurable independent of destination AMBA bus width
- 32 bit or 64 bit destination AMBA bus- user configurable independent of source AMBA bus width
- 64 destination AMBA bus address spaces
- Supports all AMBA bus transaction types
- Supports all AMBA bus burst types
- Supports AMBA bus data sizes of 1, 2, 4, and 8 bytes
- Supports all AMBA response types
- Automatic destination AMBA bus retries after RETRY and SPLIT responses on the destination AMBA bus
- Source AMBA bus transaction timeout detection, and subsequent RETRY or SPLIT response when
  - there is no room for write data
  - upon long latency read data
- Efficient use of the destination AMBA bus
  - packs write data from the source AMBA bus
  - unpacks read data from the destination AMBA bus
- Low latency and fully pipelined for highest performance
- Synchronous or asynchronous source and destination AMBA AHB bus clocks

The core is delivered as a synthesizeable RTL Verilog model. Deliverables include:

- RTL Verilog source code model of the core
- Verilog testbench and test cases
- Synthesis scripts examples
- Complete detailed documentation and training class notes