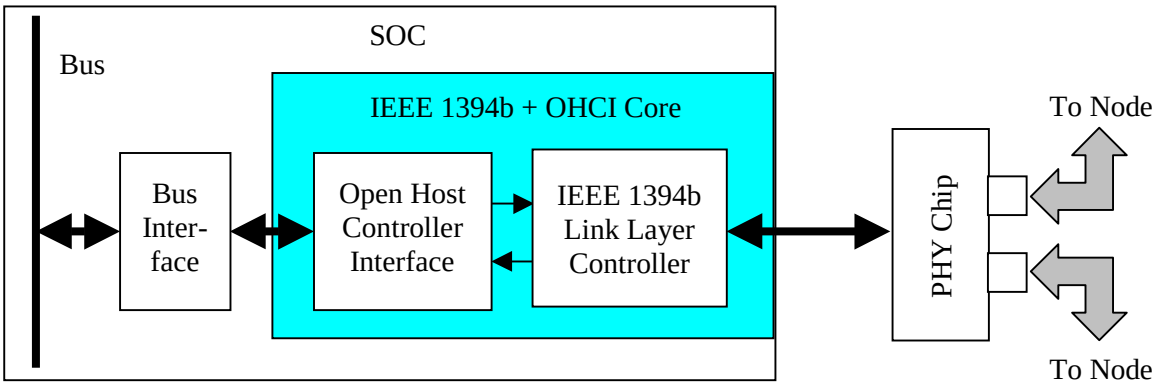
AU-F8081: IEEE 1394b + OHCI Core

The AU-F8081 IEEE 1394b + OHCI Core provides an IEEE 1394b Link Layer Controller that supports the industry standard Open Host Controller Interface (OHCI) version 1.2. OHCI is included to provide DMA packet data transfers, interrupts, and other OHCI compatible features. The figure below shows IEEE 1394b + OHCI Core usage within an SOC. The IEEE 1394b + OHCI Core is available as a synthesizable Verilog model from Aurora VLSI, Inc. Contact CustomerService@auroravlsi.com.



IEEE 1394b is a peer to peer standard. The IEEE 1394b + OHCI connects an application to the IEEE 1394b serial bus as a peer node. IEEE 1394b serial bus speeds of 100mb/s, 200mb/s, 400mb/s, 800mb/s, and 1600mb/s are supported. The IEEE 1394b Link Layer Controller block of the IEEE 1394b + OHCI Core interfaces to an external PHY using the IEEE 1394b-2002 parallel PHY standard.

Internal to an SOC, the IEEE 1394b + OHCI Core is typically a peripheral on a bus. DMA, according to the OHCI 1.2 specification, between the Open Host Controller Interface block of the IEEE 1394b + OHCI Core, and host memory targets, is used to transfer the transmit and receive data. When doing DMA, the IEEE 1394b + OHCI Core is a bus master. The IEEE 1394b + OHCI Core is also a bus master when servicing physical read and write requests to host memory, from other nodes via the PHY. The IEEE 1394b + OHCI Core is a bus slave for configuration, control, and status register accesses. Configuration, control, and status register accesses typically originate in a bus master outside of the IEEE 1394b + OHCI Core, such as a host processor.

IEEE 1394b + OHCI Core features are summarized:

IEEE 1394b Link Layer Controller

- Compliant with IEEE 1394b
- IEEE 1394b link layer functionality
- IEEE 1394b-2002 parallel PHY interface
- Supports 100, 200, 400, 800, and 1600 mbits/s
- Cycle master capability
- Generates CRC for transmit and checks CRC for receive packets
- Asynchronous and isochronous transfers are supported
- Packet status captured
- PHY status and cycle sync status

Open Host Controller Interface

- Compliant with OHCI 1.2
- 4 channel DMA Engine
  - asynchronous transmit data DMA from data source to Async Transmit FIFO
  - isochronous transmit data DMA from data source to Iso Transmit FIFO
  - asynchronous receive data DMA from Receive FIFO to data destination
  - isochronous receive data DMA from Receive FIFO to data destination
- Up to 32 isochronous transmit DMA contexts- user configurable
- Up to 32 isochronous receive DMA contexts- user configurable
- Asynchronous transmit data FIFO- 16 bytes to 32K bytes user configurable
- Isochronous transmit data FIFO- 16 bytes to 32K bytes user configurable
- Asynchronous receive data FIFO- 16 bytes to 32K bytes user configurable
- Isochronous receive data FIFO- 16 bytes to 32K bytes user configurable
- All OHCI 1.2 configuration, control, and status registers
- All OHCI 1.2 interrupts

The core is delivered as a synthesizeable RTL Verilog model. Deliverables include:

- RTL Verilog source code model of the core
- Verilog testbench and test cases
- Synthesis scripts examples
- Complete detailed documentation and training class notes

IEEE 1394b Link Layer Controller

The IEEE 1394b + OHCI Core includes the AU-F8080 IEEE 1394b Link Layer Controller (LLC) Core. Additional logic at the application interface of the IEEE 1394b LLC provides the OHCI DMA Engine and host processor interrupts for the IEEE 1394b + OHCI Core.

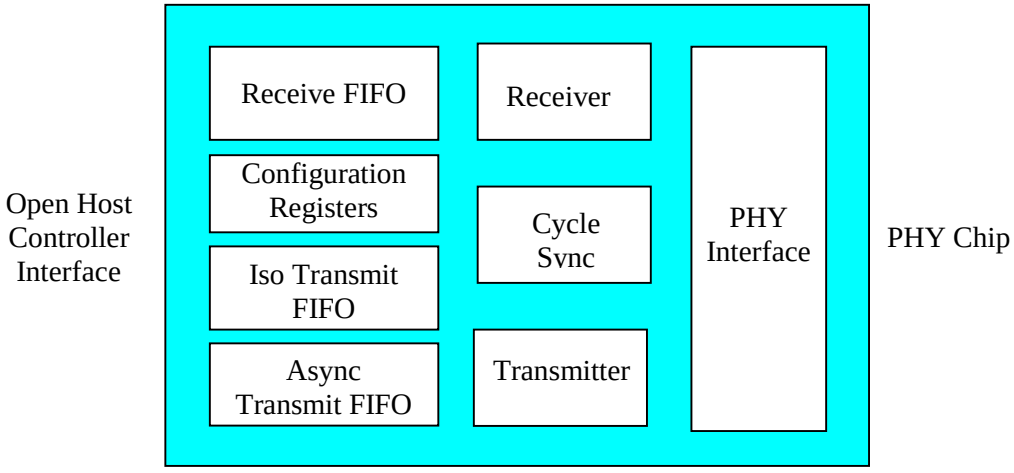
A block diagram of the IEEE 1394b LLC is shown below.

The PHY Interface provides PHY level services to the Receiver, Transmitter, and the Cycle Sync blocks. These services include gaining access to the bus, sending data packets at the required speed over the bus, receiving data packets, and sending and receiving acknowledge packets. This interface complies with the parallel PHY interface specification in the IEEE 1394b-2002 standard.

The Receiver takes the incoming data from the PHY Interface and determines if the packet is addressed to this node. If it is, it starts assembling the packet header and packet data. Both the header and the packet data are transferred to the Receive FIFO. CRC checks are performed for both the header and data packets. The CRC is not written into the Receive FIFO. During the configuration phase, the Receiver receives and processes Self-ID packets, and stores them in the Receive FIFO.

The Transmitter interfaces with the PHY Interface on one side, and with the Open Host Controller Interface through the Transmit FIFOs, on the other side. The data paths for asynchronous and isochronous transmit data are handled independently using separate FIFOs for each.

The Cycle Sync block has the cycle timer registers and counters. The IEEE 1394b LLC Core can be programmed to be the cycle master or a cycle slave. In cycle master mode, it generates cycle start packets. In cycle slave mode, it monitors the received cycle start packets.



Transmit and receive status are captured for each transmitted and received packet, respectively.

Open Host Controller Interface

The Open Host Controller Interface contains four data FIFOs to temporarily hold transmit data before sending it to the IEEE 1394b Link Layer Controller, and to temporarily hold receive data from the IEEE 1394b Link Layer Controller. Asynchronous transmit data, isochronous transmit data, asynchronous receive data, and isochronous receive data each have a dedicated data FIFO. The sizes of these FIFOs are user configurable from 16 bytes to 32K bytes.

The Open Host Controller Interface includes a four channel DMA Engine. One channel is used to transfer asynchronous transmit data from the data's source to the Async Transmit FIFO. The second channel transfers isochronous transmit data to the Iso Transmit FIFO. Asynchronous receive data is sent from the Async Receive FIFO to the received data's destination, by the third DMA channel. The fourth DMA channel is used to transfer isochronous receive data from the Iso Receive FIFO to the received data's destination.

The four DMA channels are configured and controlled by four schedulers and context processing blocks. Asynchronous transmit, isochronous transmit, asynchronous receive, and isochronous receive each have a dedicated scheduler and context processing block. The isochronous transmit and receive DMA channels support up to 32 OHCI DMA contexts each. Incoming physical requests are handled by the asynchronous receive and asynchronous transmit schedulers and context processing blocks.

A DMA operation begins when a DMA context is enabled, after the starting address and transfer count are configured in the DMA channel by its context processing block. The DMA channel moves the packet data, and the DMA operation ends when the entire packet has been moved.

The Open Host Controller Interface contains registers to configure and control the IEEE 1394b + OHCI Core, and to report its status. All OHCI 1.2 registers are included.

The Open Host Controller Interface generates interrupts to notify the host processor of events that are important to driver software. All OHCI 1.2 interrupt events are detected and signaled at the interrupt output.