AU-G0200: Timers/Counters AMBA APB Core

The AU-G0200 Timers/Counters AMBA APB Core provides a timer/counter peripheral for AMBA based SOCs. It includes eight 32 bit timers/counters connecting seamlessly to the AMBA APB Bus as an AMBA Bus slave. The Timers/Counters AMBA APB Core is available as a synthesizable Verilog model from Aurora VLSI, Inc. Contact CustomerService@auroravlsi.com.

The Timers/Counters core is configurable to contain up to eight 32 bit timers and/or counters. Each timer/counter is individually enabled by software. When enabled, it counts cycles or events according to its configuration. Each timer/counter is configurable to count by either incrementing or decrementing.

Before enabling a timer/counter, software programs its count register with its expiration count. It is then enabled and starts counting. When its count reaches the expiration count shown in its count register, an interrupt is signaled at that timer/counter's interrupt output. Alternatively, a timer/counter that is incrementing can be configured to signal an interrupt when its count rolls over. Each timer/counter can be configured to generate an interrupt pulse or a sustained interrupt that must be cleared by software. When a timer/counter signals an interrupt, depending on its configuration, it either remains enabled and starts to count to its expiration count again, or is disabled and stops counting.

Each timer/counter has a designated event input. When configured to count events, it counts each cycle that its event input is asserted. Each timer/counter's event input can be configured to be level or edge sensitive, and active high or active low.

The timers/counters can be chained together. Due to this chaining and the high degree of configurability, all typical timer/counter functions can be implemented- timer with scaled clock, timer with external clock, watchdog interrupt and reset signaling, event counting, timers with extremely long periods, one shot and periodic timers, etc.

The Timers/Counters AMBA APB Core features are summarized:

- Up to 8 timers and/or counters
- 32 bits each
- Independently enabled
- When enabled, configurable to count always (timer) or count events (counter)
- Events can be level or edge sensitive, active high or active low
- Increment or decrement (configurable)
- Interrupt upon count expiration or overflow (configurable)
- Interrupt upon expiration- interrupt pulse or continual assertion (configurable)
- Reload and continue counting, or stop upon expiration (configurable)
- Timers/counter can be chained
- Supports clock scaling for timer function, external clock for timer function, watchdog interrupt and reset signaling, and other typical timer/counter functions

The core is delivered as a synthesizeable RTL Verilog model. Deliverables include:

- RTL Verilog source code model of the core
- Verilog testbench and test cases
- Synthesis scripts examples
- Complete detailed documentation and training class notes