AU-M4000: Compact Flash Controller Core

The AU-M4000 Compact Flash Controller Core is a versatile compact flash card controller that supports CompactFlash and CF+ according to the "CF+ and CompactFlash Specification Revision 3.0". It functions in PC card memory, PC card I/O, and true IDE modes. Additionally, IDE multiword DMA and Ultra DMA are included. The Compact Flash Controller is available as a synthesizable Verilog model from Aurora VLSI, Inc. Contact CustomerService@auroravlsi.com.

The Compact Flash Controller data bus width to the compact flash card, is user configurable to 8 or 16 bits. Compact flash card timing parameters are both user configurable at reset with Verilog parameters and software programmable to support a wide range of compact flash card speed grades and system clock frequencies.

The Compact Flash Controller supports all compact flash card commands listed in the "CF+ and CompactFlash Specification Revision 3.0". In PC card modes, the host processor accesses the compact flash card common memory, attribute memory, and I/O space using the Compact Flash Controller. Additionally, the host processor may directly read and write compact flash card command block locations using the Compact Flash Controller.

The host processor initiates compact flash card operations by writing commands to the Compact Flash Controller. When a compact flash card operation completes, the Compact Flash Controller optionally signals a maskable interrupt to the host processor. The host processor may also poll Compact Flash Controller registers to determine when a compact flash card operation has completed.

Compact Flash Controller features are summarized:

- CompactFlash and CF+ version 3.0
- PC card memory, PC card I/O, and true IDE modes
- IDE multiword DMA and Ultra DMA modes
- 8 bit or 16 bit Compact Flash Controller data bus
- User configurable reset values and fully programmable compact flash card timing parameters
- Supports all compact flash card commands
- Supports direct command block accesses
- Supports common memory, attribute memory, and IO accesses (PC card modes)
- Interrupt or host processor polling for Compact Flash command completion

The core is delivered as a synthesizeable RTL Verilog model. Deliverables include:

- RTL Verilog source code model of the core
- Verilog testbench and test cases
- Synthesis scripts examples
- Complete detailed documentation and training class notes