

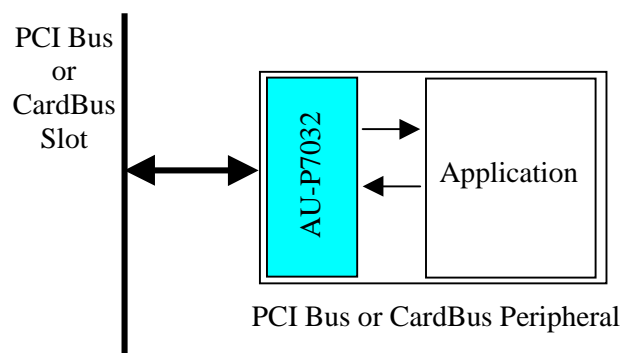
AU-P7032: 32 Bit PCI/CardBus Core

The AU-P7032 32 Bit PCI/CardBus Core provides 32 Bit PCI and CardBus master and slave functionality. PCI Bus speeds of 33MHz and 66MHz are supported. The CardBus speed is 33MHz as described by the "CardBus Specification- PC Card Standard Release 8.0". It contains the standard PCI/CardBus configuration registers including four base address registers. The 32 Bit PCI/CardBus Core is available as a synthesizable Verilog model from Aurora VLSI, Inc. Contact CustomerService@auroravlsi.com.

Features are summarized:

- PCI 2.1 and 2.2 compliant
- CardBus compliant
- Master and slave support 32 bit address and data transfers
- Supports variable burst size transfers
- Performs zero wait state transfers
- Master is capable of performing I/O, Memory, and Configuration types of PCI/CardBus transfers
- Master supports byte mode operation
- Master can perform Memory Write Invalidate and Memory Read Line operations
- Performs back to back transfers
- Includes CardBus STSCHG signal
- CardBus power management states D0, D1, D2, and D3 supported

The AU-P7032 provides a simple application interface to which any application logic can interface to a PCI Bus or CardBus slot. The application can initiate a PCI/CardBus transaction through the AU-P7032 in master mode. In slave mode, the PCI/CardBus data is written to or read from the application.



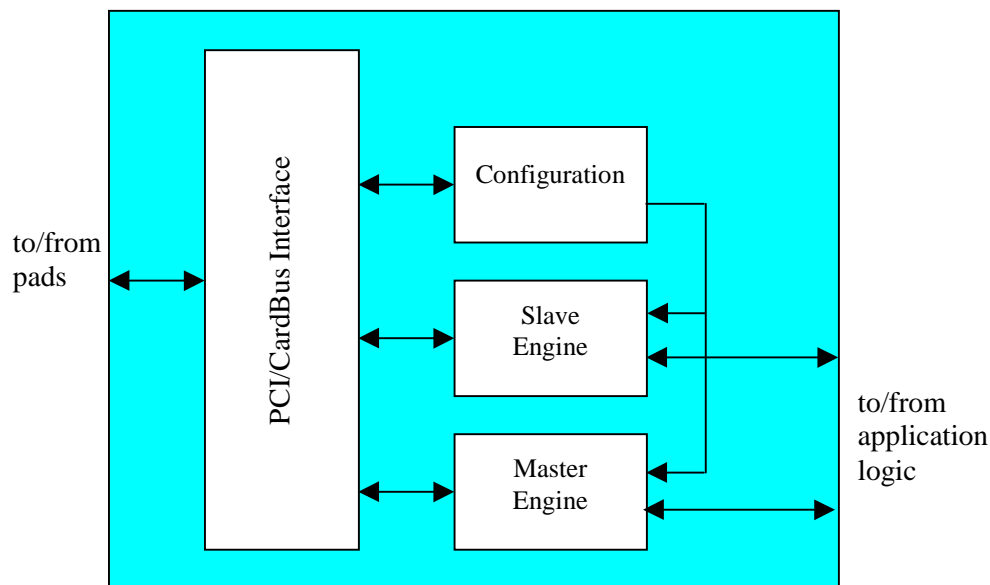
A block diagram of the AU-P7032 is shown below.

The Master Engine handles master cycles, retries, command generation, and data transfers. It also handles Memory Write Invalidate (MWI) and Memory Read Line (MRL) transfers. It generates handshake signals to communicate with the application.

The Slave Engine handles address decode, command decode, and generation of slave PCI/CardBus cycles. It is capable of performing burst transfers.

The Configuration block has the configuration address space of the AU-P7032. It is programmable to accommodate multiple base address registers. It is addressed from both the application and the slave interface.

The PCI/CardBus Interface communicates with the slave, configuration, and master data paths and address paths to generate appropriate transfers on the PCI Bus or at the CardBus slot. Pad control, data multiplexing, and parity generation and detection are performed in this block.



The core is delivered as a synthesizable RTL Verilog model. Deliverables include:

- RTL Verilog source code model of the core
- Verilog testbench and test cases
- Synthesis scripts examples
- Complete detailed documentation and training class notes