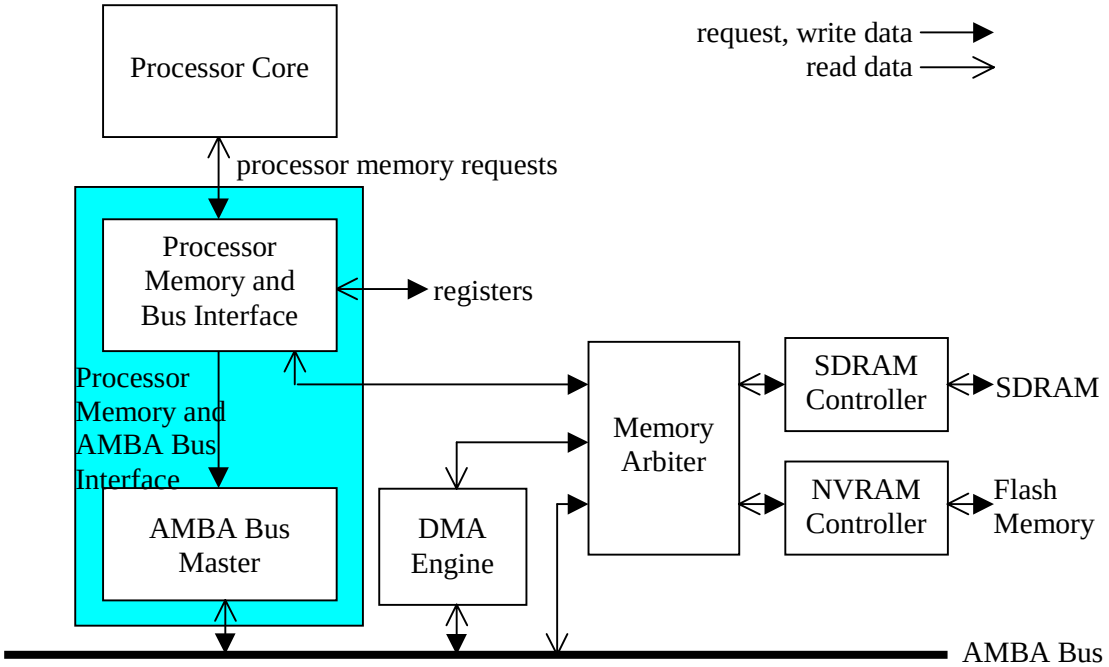
AU-SB1000: Processor Memory and AMBA Bus Interface Core

The AU-SB1000 Processor Memory and AMBA Bus Interface Core provides system interfaces for Aurora VLSI processors including the AU-C01XX Processor Core family and AU-JXXXX Java Core family, in AMBA based SOCs. In an SOC, it connects the Processor Core to the memory system that may include RAM, an AMBA AHB Bus, and on-chip configuration, control, and status registers. The AU-SB1000 Processor Memory and AMBA Bus Interface Core is available as synthesizable Verilog models from Aurora VLSI, Inc. Contact CustomerService@auroravlsi.com.

The Processor Memory and AMBA Bus Interface Core is a block at the Processor Core to memory system interface. It seamlessly connects the Processor Core to the memory system. The figure below shows its usage within an SOC.



The Processor Core initiates memory system requests that may go to RAM, AMBA Bus peripherals, or on-chip configuration, control, and status registers. The request address identifies the request target. The Processor Memory and AMBA Bus Interface decodes the request address and drives signals at its on-chip register interface, at its RAM interface, or onto the AMBA Bus, as determined by the request address.

When an AMBA Bus request is detected, the Processor Core is effectively the AMBA Bus Master, as the request is driven onto the AMBA Bus by the Processor Memory and AMBA Bus Interface Core.

Processor Memory and AMBA Bus Interface features are summarized:

Processor Memory and Bus Interface

- Memory and bus interface supporting Aurora VLSI Processor Cores
  - AU-C01XX 32 Bit, Tiny, Low Power Processor Cores
  - AU-JXXXX Java Processor Cores
- Seamless connection to Aurora VLSI Processor Cores
- Memory system requests from the Processor Core on two independent request interfaces
  - instruction request interface
  - data request interface
- Determines the memory request target:
  - RAM memory
  - AMBA Bus peripheral device
  - On-chip register
- Drives the request to the memory request target
- Receives read data and error information from the request target
- Passes read data and error information back to the Processor Core
- Signals memory system wait cycles to the Processor Core as needed

AMBA Bus Master

- 32 bit or 64 bit AMBA AHB Bus- user configurable
- Fully pipelined for highest throughput
- Supports all required AMBA AHB Bus features
- AMBA Bus read error returned to the user with the read data

The core is delivered as a synthesizeable RTL Verilog model. Deliverables include:

- RTL Verilog source code model of the core
- Verilog testbench and test cases
- Synthesis scripts examples
- Complete detailed documentation and training class notes

Processor Memory and Bus Interface

The Processor Memory and AMBA Bus Interface includes the AU-S1000 Processor Memory and Bus Interface Core. Additional logic at the bus interface of the Processor Memory and Bus Interface Core provides an AMBA Bus Master interface for the Processor Memory and AMBA Bus Interface.

The Processor Core issues memory requests on its instruction and data memory interfaces. These two Processor Core memory request interfaces operate independently. The Processor Memory and Bus Interface receives these requests, and examines each request address to determine if it is a request for:

- RAM memory
- A AMBA Bus peripheral device
- A control or status register within the memory system

It then passes the request information- request address, size, read/write, lock flag, and any write data, to the memory system block that controls the appropriate request target- RAM memory, AMBA Bus, or SOC internal control and status registers.

On Processor Core reads, some time after passing the request information to the appropriate request target block, the Processor Memory and Bus Interface receives the read data and error information from the request target block. It then passes this read data and error information back to the Processor Core. The Processor Memory and Bus Interface signals wait cycles to the Processor Core as it waits for the read data and error information.

On Processor Core writes, the Processor Memory and Bus Interface accepts write data with the request. It then passes the write data along with the request to the appropriate memory system target.

AMBA Bus Master

The AMBA Bus Master can connect to either a 32 bit or 64 bit AMBA AHB Bus. A Verilog parameter indicates the AMBA Bus width.

The AMBA Bus Master is fully pipelined for highest throughput, and therefore highest system performance. It can issue AMBA Bus requests, drive AMBA Bus data, and capture data from the AMBA Bus, each AMBA Bus clock cycle.

The AMBA Bus Master supports all required AMBA AHB Bus features including all AMBA burst and wrapping types, AMBA sizes up to the AMBA Bus width, and the AMBA Bus lock feature. Request lengths of up to 32 Kbytes from the user are supported and translated into one or more AMBA Bus transactions. When an AMBA slave responds with the RETRY or SPLIT response, the AMBA Bus Master responds accordingly to eventually complete the transaction. This is transparent to the user (accept for the additional delay).

The Processor Memory and Bus Interface block issues AMBA Bus requests to the AMBA Bus Master. After accepting a request, the AMBA Bus Master initiates and completes an AMBA Bus transaction for the accepted request. The AMBA Bus Master interfaces directly onto the AMBA bus and takes care of all AMBA Bus protocol requirements for the transaction. If the transaction is a read transaction, the AMBA Bus Master assembles the read data from the AMBA Bus and returns it to the Processor Memory and Bus Interface block.

The AMBA Bus Master also returns read errors from the AMBA Bus. The read error from a slave's ERROR response, is returned along with the read data that came with the slave's ERROR response. The user interprets the read data that came with the read error according to the slave's definition of read data with the ERROR response. Slave ERROR responses upon AMBA Bus writes are not returned to the user. Writes fail silently.