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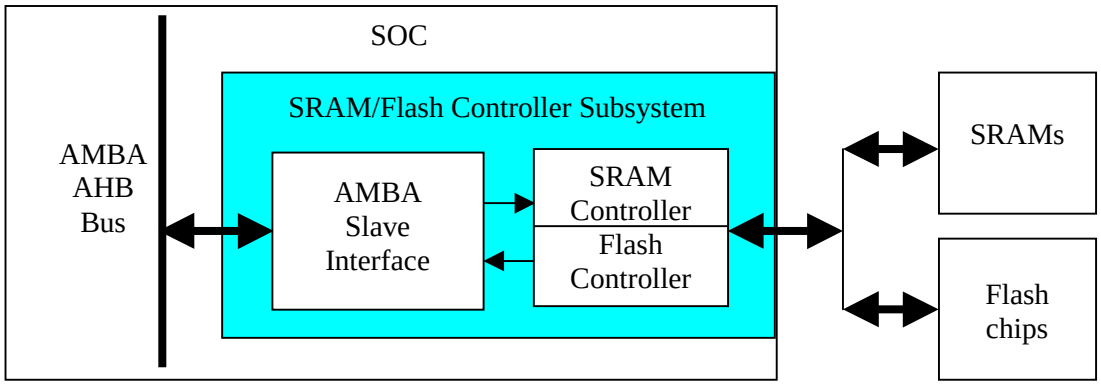
AU-SS1000: SRAM/Flash Controller AMBA Subsystem Core

AMBA AHB Bus SRAM/Flash Controller

The AU-SS1000 SRAM/Flash Controller AMBA Subsystem provides an SRAM and flash controller subsystem for AMBA based SOCs. It contains an SRAM controller and NAND/NOR flash controller that connect seamlessly to the AMBA AHB bus as an AMBA Bus slave. The SRAM/Flash Controller AMBA Subsystem Core is available as a synthesizable Verilog model from Aurora VLSI, Inc. Contact CustomerService@auroravlsi.com.



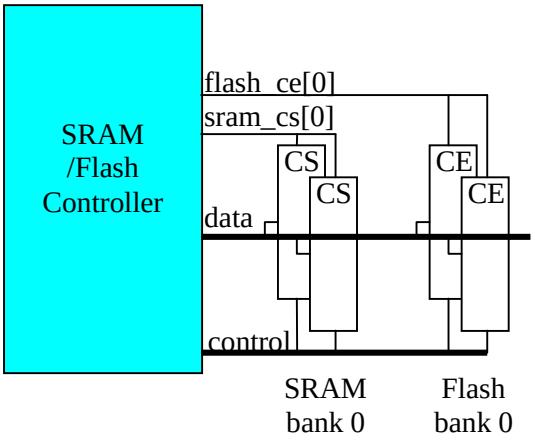
Systems that include the SRAM/Flash Controller Subsystem can be built with two types of memory:

- SRAM
- NAND or NOR flash chips- pin strapping configures the Flash Controller

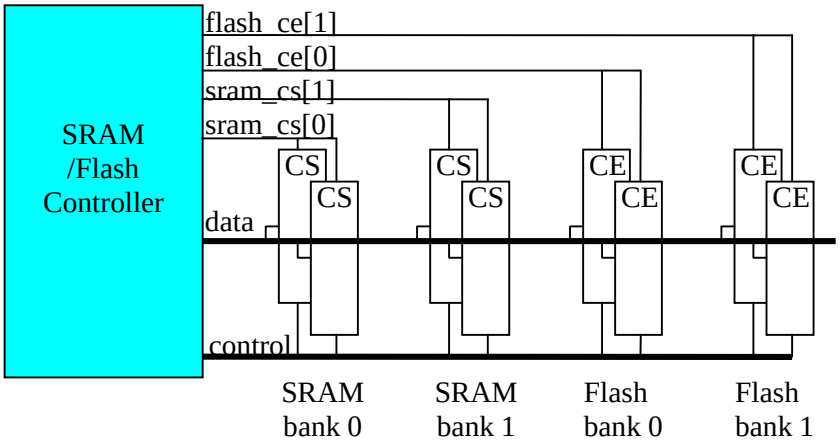
The data bus to the SRAMs is user configurable to 32 or 64 bits. The flash data bus can be configured to 8, 16, 32, or 64 bits. To minimize pin count, the SRAM and flash chip interfaces share the data bus. Chip select lines, other control lines, and the SRAM clock are dedicated signals, as opposed to being shared signals.

The SRAM/Flash Controller Subsystem supports one, two, or four SRAM banks through its SRAM chip select outputs- sram_cs[3:0], and one, two, or four banks of flash chips with its flash chip enable outputs- flash_ce[3:0]. The data bus is used by both the SRAMs and flash chips. The SRAM clock and control lines are common to all banks of SRAM. Flash control lines and the flash chip ready signal are shared by the flash chips.

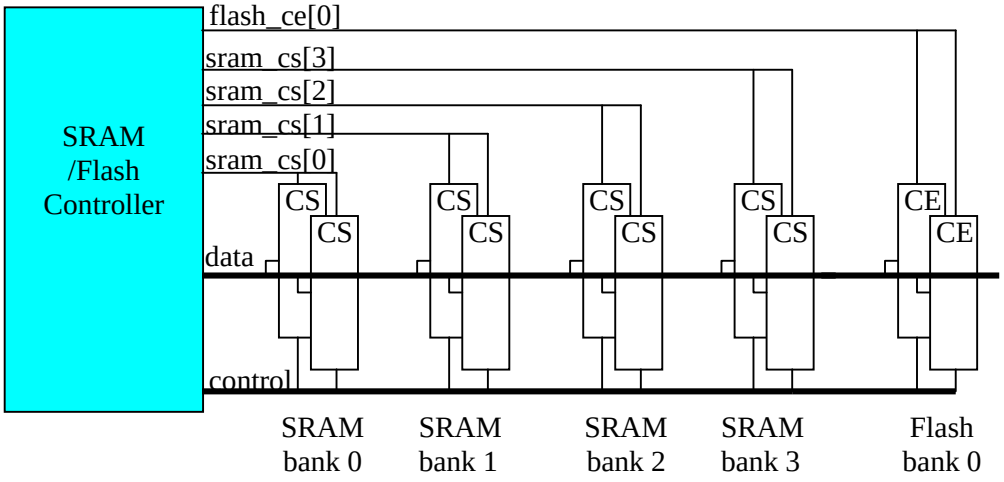
The figures below show some of the possible memory systems that can be built with the SRAM/Flash Controller Subsystem.



One SRAM Bank and One Flash Bank



Two SRAM Banks and Two Flash Banks



Four SRAM Banks and One Flash Bank

A versatile, pipelined, high performance SRAM Controller is included in the SRAM/Flash Controller Subsystem.. Several SRAM types are supported including flow through ZBT synchronous SRAMs, pipelined ZBT synchronous SRAMs, flow through syncburst synchronous SRAMs, SCD syncburst synchronous SRAMs, DCD syncburst synchronous SRAMs, and asynchronous SRAMs. The SRAM Controller supports SRAM memory systems from 512 Kbytes to 512 Mbytes. The SRAM data bus width is user configurable to 32 or 64 bits. To conserve power the SRAMs can be put in low power mode.

The SRAM/Flash Controller Subsystem includes a versatile NAND/NOR flash controller that supports various types of NAND and NOR flash chips from several manufacturers. The Flash Controller supports NAND flash memory systems from 8 Mbytes to 16 Gbytes, and NOR flash memory systems from 512 Kbytes to 1 Gbyte. Flash chip timing parameters are both user configurable at reset with Verilog parameters and software programmable to support a wide range of flash speed grades and system clock frequencies.

Internal to an SOC, the SRAM/Flash Controller Subsystem is a bus slave peripheral on the AMBA AHB Bus. The SRAM/Flash Controller Subsystem can interface to either a 32 bit or 64 bit AMBA AHB Bus. A Verilog parameter indicates the AMBA Bus width. The host processor configures, controls, and checks status of the SRAM/Flash Controller Subsystem by doing AMBA Bus transactions to the register slave address space. The SRAM slave address space is used to transfer data to and from the SRAMs. Data is transferred to and from the flash chips using the flash slave address space.

SRAM/Flash Controller AMBA Subsystem features are summarized:

- SRAM controller and interface
- NAND flash controller and interface
- NOR flash controller and interface
- All interfaces share chip pins for reduced pin count
- 32 or 64 bit AMBA AHB Bus interface- user configurable
- AMBA Bus slave

SRAM Controller

- Supports several SRAM types- flow through ZBT synchronous, pipelined ZBT synchronous, flow through syncburst synchronous, SCD syncburst synchronous, DCD syncburst synchronous, and asynchronous SRAMs
- 32 bit or 64 bit SRAM data bus
- 512 Kbyte to 512 Mbyte SRAM memory system
- Pipelined accesses for highest performance
- 0, 1, or 2 cycle read latency
- 0, 1, or 2 cycle write latency
- 1, 2, or 4 banks of SRAM
- 17 to 24 address bits
- SRAM powerdown supported

Flash Controller

- NAND and NOR flash controller
- 1, 2, or 4 banks of flash chips
- 8 bit, 16 bit, 32 bit, or 64 bit Flash Controller data bus
- 8 Mbyte to 16 Gbyte NAND flash memory systems
- 512 Kbyte to 1 Gbyte NOR flash memory systems
- User configurable reset values and fully programmable flash chip timing parameters
- NAND flash
  - Read, Program, Erase, Read Status, Read ID, Copy Back, and Reset
  - 64 Mbit to 8 Gbit flash chips- configurable
  - 8 bit or 16 bit flash chip data bus- configurable
  - 512 byte or 2048 byte page size- configurable
  - ECC generation and correction
  - spare area usage- configurable
  - 2 or 4 cycle ID register read- configurable
- NOR flash
  - Read, Program, Erase, Read Status, Read ID, Read CFI, Clear Status, Buffered Write, Lock, Unlock, and Lock Down
  - 4 Mbit to 512 Mbit flash chips- configurable
  - 8 bit or 16 bit flash chip data bus- configurable
  - 64 Kbyte or 128 Kbyte main block size- configurable
  - top, bottom, or no boot block- configurable
  - 8 Kbyte, 16 Kbyte, or 32 Kbyte boot block size- configurable
- Interrupt or host processor polling for flash command completion

AMBA Slave Interface

- AMBA AHB Bus slave
- 32 bit or 64 bit AMBA AHB Bus- user configurable
- Supports all required AMBA AHB Bus features
- Implements AMBA Bus timeout and RETRY response
- Read data prefetching
- Write data packing
- Same cycle device request/response is supported for highest throughput
- Handles all data packing/unpacking and data alignment for data transfer sizes that do not match the AMBA Bus width and/or SRAM/flash data bus width
- User configurable for big or little endian AMBA Bus and memory
- AMBA Bus and SRAM interface can be asynchronous to each other

The core is delivered as a synthesizeable RTL Verilog model. Deliverables include:

- RTL Verilog source code model of the core
- Verilog testbench and test cases
- Synthesis scripts examples
- Complete detailed documentation and training class notes

SRAM Controller

The SRAM/Flash Controller Subsystem includes the AU-M1000 SRAM Controller Core. Additional logic at the requester interface of the SRAM Controller provides an AMBA Bus slave interface, read prefetching logic, and write data packing.

The SRAM Controller accepts SRAM requests and converts them into pipelined SRAM accesses within the SRAM Controller. This results in a peak bandwidth of 4 bytes/cycle with a 32 bit SRAM data bus, and 8 bytes/cycle with a 64 bit SRAM data bus. The SRAM Controller ensures that correct latencies and bus turn around times are met.

The number of SRAM address bits and SRAM banks is software configurable. Seventeen to twenty four address bits are supported. One, two, or four banks of SRAM can be built into the system. The SRAM chip select pins are used to identify the accessed bank of SRAM. This flexibility permits SRAM memory system of 512 Kbytes to 512 Mbytes.

SRAM read and write latencies are software programmable. This allows the SRAM Controller to be used with a wide variety of SRAMs. Asynchronous SRAMs and many types of synchronous SRAMs are supported.

Upon reset, SRAM accesses are optionally enabled or disabled according to a user configurable Verilog parameter. Software may also enable and disable SRAM accesses. Read and write latencies, the number of address bits, and number of SRAM banks are also user configurable upon reset with Verilog parameters. After reset de-assertion, software may overwrite the read and write latencies, number of address bits, and number of SRAM bank reset values.

The user may put the SRAMs into low power mode through software. Low power mode is exited when a read/write request occurs or when software exits low power mode.

Flash Controller

The SRAM/Flash Controller Subsystem includes the AU-M3000 Flash Controller Core. Additional logic at the requester interface of the Flash Controller provides an AMBA Bus slave interface, read prefetching logic, and write data packing.

The Flash Controller supports the Read, Program, Erase, Read Status, Read ID, Copy Back, and Reset NAND flash commands. ECC generation and correction is provided for NAND flash systems. NOR flash commands that are supported include Read, Program, Erase, Read Status, Read ID, Read CFI, Clear Status, Buffered Write, Lock, Unlock, and Lock Down.

In NAND flash systems, configurable features include page size, data bus width, flash chip size, number of flash banks, interrupt enable, ECC functionality, copy back functionality, command confirmation, number of address cycles, number of ID read cycles, spare area usage, and address[33:32]. Configurable features for NOR flash systems include, data bus width, flash chip size, number of flash banks, interrupt enable, block size, boot block configuration, lock feature, burst read feature, buffered write feature, and the CFI feature. Configurable features have hardwired values upon reset that are user configurable with Verilog parameters. After reset, they can be reconfigured by software.

Flash timing parameters at reset are hardwired to user configurable values. After reset, they are software programmable. This allows the Flash Controller to be used for boot code at reset with a wide range of flash speed grades and system cycle times. After booting, performance can be optimized by reconfiguring the flash timing parameters for the specific flash chips that are used and the system clock frequency.

The host processor initiates flash chip operations by writing commands to the Flash Controller. When a flash chip operation completes, the Flash Controller optionally signals a maskable interrupt to the host processor. The host processor may also poll Flash Controller registers to determine when a flash chip operation has completed.

AMBA Slave Interface

The AMBA Slave Interface of the SRAM/Flash Controller Subsystem, accepts SRAM, flash, and register requests from the AMBA Bus. The AMBA Slave Interface supports all required AMBA AHB Bus features including all AMBA burst and wrapping types, AMBA sizes up to the AMBA Bus width, and all AMBA Bus responses. When the AMBA Bus data transfer size does not match the AMBA Bus width or SRAM/flash data bus width the AMBA Slave Interface packs and/or unpacks the data and aligns the data, for the most efficient transfer of data to/from the SRAMs or flash chips, and to/from the AMBA Bus.

The AMBA Slave Interface can respond in the cycle after it receives an AMBA Bus request. This ensures a slave response on the AMBA Bus with no wait states, and therefore highest system performance. To support this fast response time, read data is prefetched whenever possible.

Typically, the SRAMs and the AMBA Bus do not run at the same clock rate. The AMBA Bus and SRAM interface can be completely asynchronous to each other due to the two independent clock domains of the SRAM/Flash Controller Subsystem. One clock domain includes the AMBA Bus interface logic. The SRAM interface logic is in the second clock domain. These two clock domains come together in the AMBA Slave Interface block. Each clock domain has its own SRAM/Flash Controller Subsystem clock input.

NAND flash chips provide ECC support by including spare memory areas to hold ECC bits. The SRAM/Flash Controller Subsystem can be configured to use this ECC support and do error checking and correction of the single bit correctable errors. This error checking and correction is done in the AMBA Slave Interface.