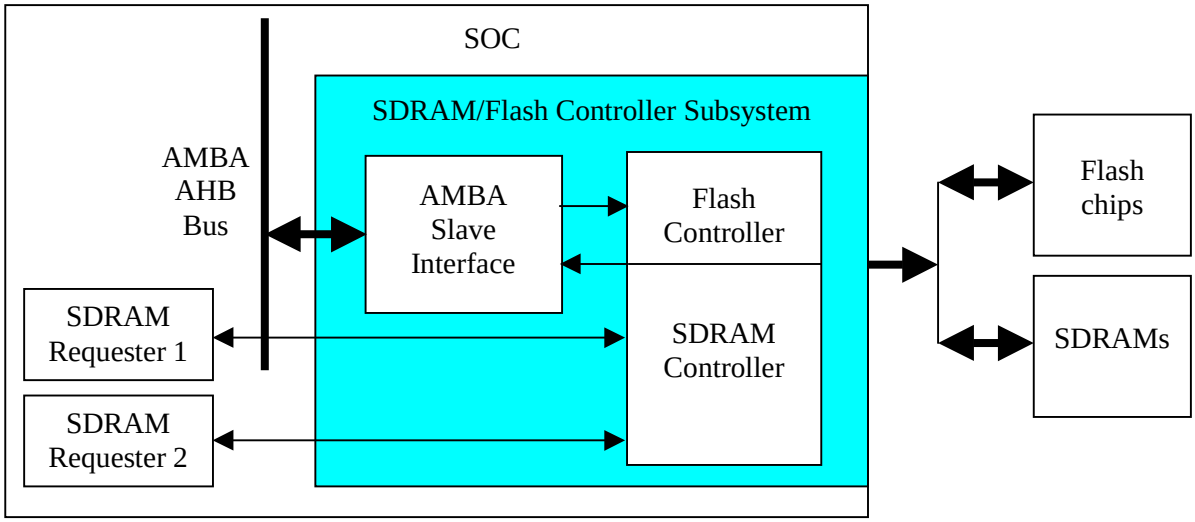
AU-SS2001: 3 Port SDRAM/Flash Controller AMBA Subsystem Core

AMBA AHB Bus SDRAM/Flash Controller

The AU-SS2001 SDRAM/Flash Controller AMBA Subsystem provides a three port SDRAM controller and single port flash controller subsystem for AMBA based SOCs. It contains an SDRAM controller and NAND/NOR flash controller that connect seamlessly to the AMBA AHB Bus as an AMBA Bus slave. It also has two additional generic SDRAM request ports. The SDRAM/Flash Controller AMBA Subsystem Core is available as a synthesizable Verilog model from Aurora VLSI, Inc. Contact CustomerService@auroravlsi.com.



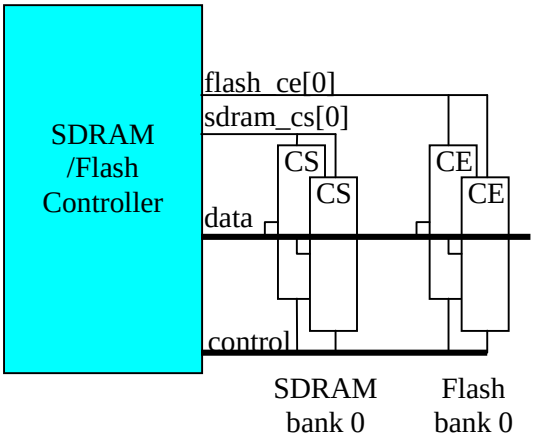
Systems that include the SDRAM/Flash Controller Subsystem can be built with two types of memory:

- SDRAM
- NAND or NOR flash chips- pin strapping configures the Flash Controller

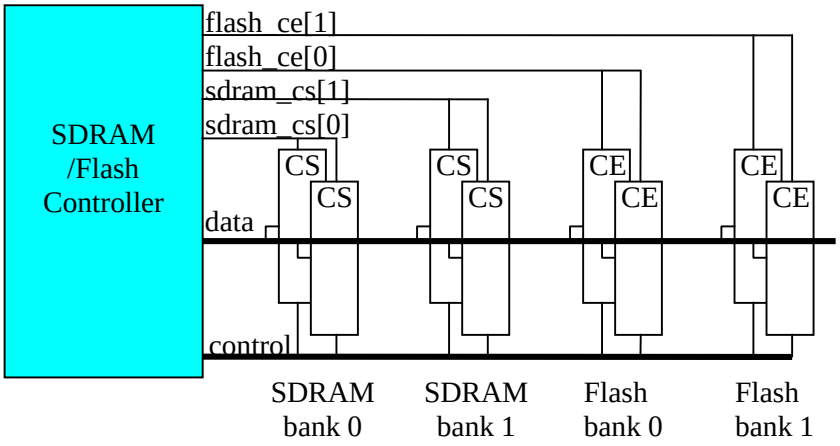
The data bus to the SDRAMs is user configurable to 32 or 64 bits. The flash data bus can be configured to 8, 16, 32, or 64 bits. To minimize pin count, the SDRAM and flash chip interfaces share the data bus. Chip select lines, other control lines, and the SDRAM clock are dedicated signals, as opposed to being shared signals.

The SDRAM/Flash Controller Subsystem supports one, two, or four SDRAM banks (external SDRAM banks) through its SDRAM chip select outputs- sdram_cs[3:0], and one, two, or four banks of flash chips with its flash chip enable outputs- flash_ce[3:0]. The data bus is used by both the SDRAMs and flash chips. The SDRAM clock enable signal, clock, and SDRAM control lines are common to all banks of SDRAM. Flash control lines and the flash chip ready signal are shared by the flash chips.

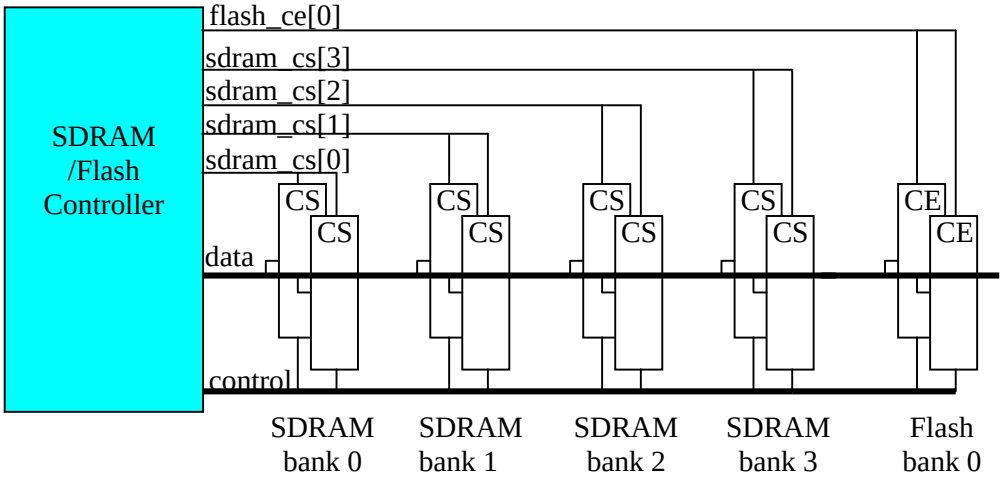
The figures below show some of the possible memory systems that can be built with the SDRAM/Flash Controller Subsystem.



One SDRAM Bank and One Flash Bank



Two SDRAM Banks and Two Flash Banks



Four SDRAM Banks and One Flash Bank

A pipelined, high performance SDRAM Controller is included in the SDRAM/Flash Controller Subsystem. The SDRAM Controller supports SDRAM memory systems from 4 Mbytes to 4 Gbytes. SDRAM timing parameters are software programmable to support a wide range of SDRAM speed grades and clock frequencies. Refresh is initiated by the SDRAM Controller according to the software programmable refresh interval. To conserve power the SDRAMs can be put in low power mode.

The SDRAM/Flash Controller Subsystem includes a versatile NAND/NOR flash controller that supports various types of NAND and NOR flash chips from several manufacturers. The Flash Controller supports NAND flash memory systems from 8 Mbytes to 16 Gbytes, and NOR flash memory systems from 512 Kbytes to 1 Gbyte. Flash chip timing parameters are both user configurable at reset with Verilog parameters and software programmable to support a wide range of flash speed grades and system clock frequencies.

Internal to an SOC, the SDRAM/Flash Controller Subsystem is a bus slave peripheral on the AMBA AHB Bus. The SDRAM/Flash Controller Subsystem can interface to either a 32 bit or 64 bit AMBA AHB Bus. A Verilog parameter indicates the AMBA Bus width. The host processor configures, controls, and checks status of the SDRAM/Flash Controller Subsystem by doing AMBA Bus transactions to the register slave address space. The SDRAM slave address space is used to transfer data to and from the SDRAMs. Data is transferred to and from the flash chips using the flash slave address space.

SDRAM/Flash Controller AMBA Subsystem features are summarized:

- SDRAM controller and interface
- NAND flash controller and interface
- NOR flash controller and interface
- All interfaces share chip pins for reduced pin count
- 32 or 64 bit AMBA AHB Bus interface- user configurable
- AMBA Bus slave
- 2 generic SDRAM request interfaces

SDRAM Controller

- 32 bit or 64 bit SDRAM data bus
- 4 Mbyte to 4 Gbyte SDRAM memory system
- Pipelined accesses to active rows for highest performance
- 2 or 3 cycle CAS latency
- 1, 2, or 4 banks of SDRAM
- 2 or 4 SDRAM internal banks
- 8, 9, 10, 11, or 12 column address bits
- 11, 12, or 13 row address bits
- SDRAM powerdown supported
- Fully programmable SDRAM timing parameters
- Auto-refresh with programmable SDRAM refresh interval

Flash Controller

- NAND and NOR flash controller
- 1, 2, or 4 banks of flash chips
- 8 bit, 16 bit, 32 bit, or 64 bit Flash Controller data bus
- 8 Mbyte to 16 Gbyte NAND flash memory systems
- 512 Kbyte to 1 Gbyte NOR flash memory systems
- User configurable reset values and fully programmable flash chip timing parameters
- NAND flash
  - Read, Program, Erase, Read Status, Read ID, Copy Back, and Reset
  - 64 Mbit to 8 Gbit flash chips- configurable
  - 8 bit or 16 bit flash chip data bus- configurable
  - 512 byte or 2048 byte page size- configurable
  - ECC generation and correction
  - spare area usage- configurable
  - 2 or 4 cycle ID register read- configurable
- NOR flash
  - Read, Program, Erase, Read Status, Read ID, Read CFI, Clear Status, Buffered Write, Lock, Unlock, and Lock Down
  - 4 Mbit to 512 Mbit flash chips- configurable
  - 8 bit or 16 bit flash chip data bus- configurable
  - 64 Kbyte or 128 Kbyte main block size- configurable
  - top, bottom, or no boot block- configurable
  - 8 Kbyte, 16 Kbyte, or 32 Kbyte boot block size- configurable
- Interrupt or host processor polling for flash command completion

AMBA Slave Interface

- AMBA AHB Bus slave
- 32 bit or 64 bit AMBA AHB Bus- user configurable
- Supports all required AMBA AHB Bus features
- Implements AMBA Bus timeout and RETRY response
- Read data prefetching
- Write data packing
- Same cycle device request/response is supported for highest throughput
- Handles all data packing/unpacking and data alignment for data transfer sizes that do not match the AMBA Bus width and/or SDRAM/flash data bus width
- User configurable for big or little endian AMBA Bus and memory
- AMBA Bus and SDRAM interface can be asynchronous to each other

The core is delivered as a synthesizeable RTL Verilog model. Deliverables include:

- RTL Verilog source code model of the core
- Verilog testbench and test cases
- Synthesis scripts examples
- Complete detailed documentation and training class notes

SDRAM Controller

The SDRAM/Flash Controller Subsystem includes the AU-M2000 SDRAM Controller Core. Additional logic at the requester interface of the SDRAM Controller provides an AMBA Bus slave interface, read prefetching logic, and write data packing.

The SDRAM Controller accepts SDRAM requests from the AMBA Slave Interface, and compares the request address to addresses of all active rows. If the request address falls in an active row, the request goes directly to the SDRAMs without stalling the SDRAM Controller pipeline. This results in a peak bandwidth of 4 bytes/cycle with a 32 bit SDRAM data bus, and 8 bytes/cycle with a 64 bit SDRAM data bus. Once a row is activated, it is left activated so that the maximum amount of requests are to active rows, resulting in highest performance.

The number of row address bits, column address bits, bank address bits, and the SDRAM banks is software configurable. Eight to twelve column address bits are supported. The number of row address bits can be set to eleven, twelve, or thirteen. SDRAMs with either two or four internal banks are supported. One, two, or four banks of SDRAM (external banks) can be built into the system. The SDRAM chip select pins are used to identify the accessed bank of SDRAM. This flexibility permits SDRAM memory system of 4 Mbytes to 4 Gbytes.

SDRAM timing parameters are software programmable. This allows the SDRAM Controller to be used with a wide range of SDRAM speed grades and cycle times. CAS latency is also software programmable.

The SDRAM refresh interval is software programmable. Each time the refresh interval expires, the SDRAM Controller performs an auto-refresh cycle to all SDRAM internal and external banks.

Upon reset, SDRAM accesses are disabled. After programming the SDRAM Controller registers to configure the SDRAM system- sizes, timing parameters, CAS latency, etc., software enables SDRAM accesses. Once enabled, the SDRAM controller loads the SDRAMs' Mode Registers, performs the appropriate refresh cycles, and is then ready to accept SDRAM read and write requests.

The user may put the SDRAMs into low power mode through software. The SDRAM Controller continues to initiate refresh cycles while the SDRAMs are powered down. Low power mode is exited when a read/write request occurs or when software exits low power mode.

Flash Controller

The SDRAM/Flash Controller Subsystem includes the AU-M3000 Flash Controller Core. Additional logic at the requester interface of the Flash Controller provides an AMBA Bus slave interface, read prefetching logic, and write data packing.

The Flash Controller supports the Read, Program, Erase, Read Status, Read ID, Copy Back, and Reset NAND flash commands. ECC generation and correction is provided for NAND flash systems. NOR flash commands that are supported include Read, Program, Erase, Read Status, Read ID, Read CFI, Clear Status, Buffered Write, Lock, Unlock, and Lock Down.

In NAND flash systems, configurable features include page size, data bus width, flash chip size, number of flash banks, interrupt enable, ECC functionality, copy back functionality, command confirmation, number of address cycles, number of ID read cycles, spare area usage, and

address[33:32]. Configurable features for NOR flash systems include, data bus width, flash chip size, number of flash banks, interrupt enable, block size, boot block configuration, lock feature, burst read feature, buffered write feature, and the CFI feature. Configurable features have hardwired values upon reset that are user configurable with Verilog parameters. After reset, they can be reconfigured by software.

Flash timing parameters at reset are hardwired to user configurable values. After reset, they are software programmable. This allows the Flash Controller to be used for boot code at reset with a wide range of flash speed grades and system cycle times. After booting, performance can be optimized by reconfiguring the flash timing parameters for the specific flash chips that are used and the system clock frequency.

The host processor initiates flash chip operations by writing commands to the Flash Controller. When a flash chip operation completes, the Flash Controller optionally signals a maskable interrupt to the host processor. The host processor may also poll Flash Controller registers to determine when a flash chip operation has completed.

SDRAM Generic Requester Interface

In addition to the AMBA Bus requester, two other SDRAM users can access SDRAM through the two independent Generic SDRAM Requester Interfaces of the SDRAM/Flash Controller Subsystem. Each of these Generic SDRAM Request Interfaces has a simple request/ready protocol to issue SDRAM requests to the SDRAM Controller. Write data is sent to the SDRAM Controller using a simple valid/ready protocol. A valid/ready protocol is also used to return read data to the requester.

AMBA Slave Interface

The AMBA Slave Interface of the SDRAM/Flash Controller Subsystem, accepts SDRAM, flash, and register requests from the AMBA Bus. The AMBA Slave Interface supports all required AMBA AHB Bus features including all AMBA burst and wrapping types, AMBA sizes up to the AMBA Bus width, and all AMBA Bus responses. When the AMBA Bus data transfer size does not match the AMBA Bus width or SDRAM/flash data bus width the AMBA Slave Interface packs and/or unpacks the data and aligns the data, for the most efficient transfer of data to/from the SDRAMs or flash chips, and to/from the AMBA Bus.

The AMBA Slave Interface can respond in the cycle after it receives an AMBA Bus request. This ensures a slave response on the AMBA Bus with no wait states, and therefore highest system performance. To support this fast response time, read data is prefetched whenever possible.

Typically, the SDRAMs and the AMBA Bus do not run at the same clock rate. The AMBA Bus and SDRAM interface can be completely asynchronous to each other due to the two independent clock domains of the SDRAM/Flash Controller Subsystem. One clock domain includes the AMBA Bus interface logic. The SDRAM interface logic is in the second clock domain. These two clock domains come together in the AMBA Slave Interface block. Each clock domain has its own SDRAM/Flash Controller Subsystem clock input.

NAND flash chips provide ECC support by including spare memory areas to hold ECC bits. The SDRAM/Flash Controller Subsystem can be configured to use this ECC support and do error checking and correction of the single bit correctable errors. This error checking and correction is done in the AMBA Slave Interface.