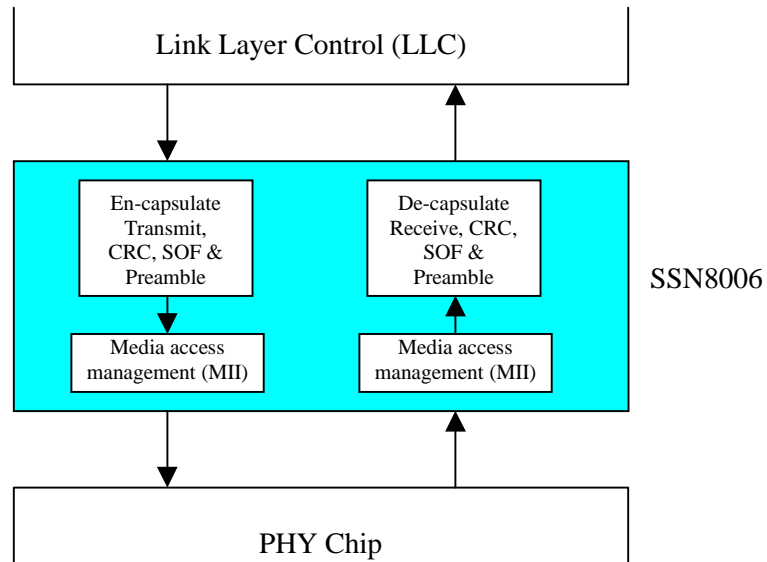




SSN8006: Ethernet 10/100 MAC Core

The SSN8006 is an Ethernet 10/100mb/s Media Access Controller. It performs the IEEE 802.3 recommended service specification for Media Access Control. A block representation of SSN8006 as per the IEEE standard specifications is shown below. The Ethernet 10/100 MAC Core is available as a synthesizable Verilog model from Aurora VLSI, Inc. Contact CustomerService@auroravlsi.com.



Transmit data is transferred from the LLC to the SSN8006. The SSN8006 packages the data, including Preamble, SOF, PAD bytes as needed, and FCS. When the transmitter is not in the deferred mode, packets are transmitted to the PHY. The industry standard MII (or RMII) interface is used to transfer the packet to the PHY chip. Upon each frame transmission, the transmit status is transferred back to the application.

Received data is checked for size and FCS correctness, and its destination address is filtered. Then if it passes address filtering, the received data is transferred to the LLC. If the length field in the frame is less than the minimum frame size, the PAD bytes are stripped from the frame. All of these operations can be enabled or disabled through the SSN8006 configuration registers. When a frame is received, its receive status is also transferred to the application.

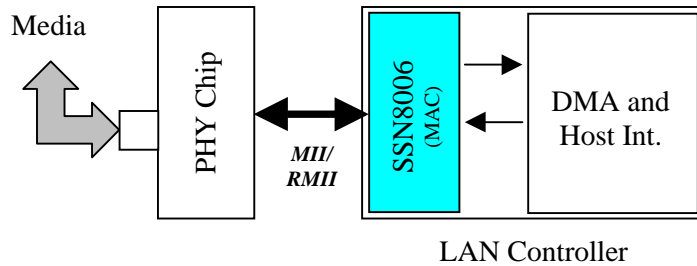
Features are summarized:

- Simple request/acknowledge interface to the application logic
- IEEE 802.3 compatible, supports IEEE 802.3x and IEEE 802.3Q for flow control
- Optional two-part deferral implemented
- Full and half duplex
- Automatic retries after collision, programmable retry counter
- Automatic padding and removal of PAD bytes to meet minimum frame size
- Industry standard MII or RMII interface to the PHY
- FCS generation for transmitted packets, and checking on received packets
- MDIO interface for PHY management
- Programmable address filtering

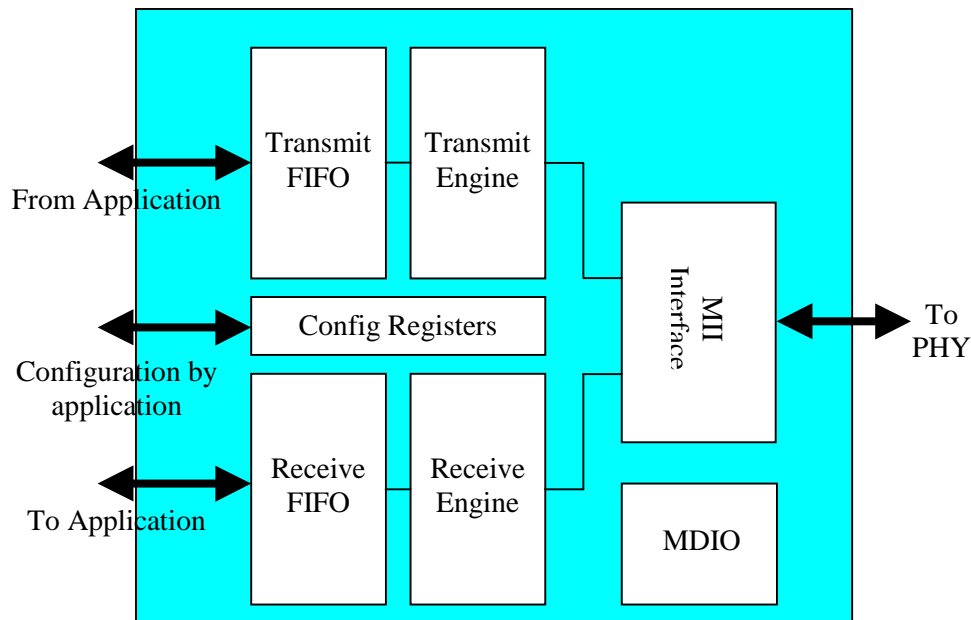


Use of the SSN8006 Ethernet 10/100 MAC Core is shown below. The PHY interface is the industry standard Media Independent Interface (MII) or Reduced Media Independent Interface (RMII), as determined by a configuration register.

The interface between the application and the SSN8006 is a simple, easy to use FIFO interface. The sizes of the Transmit FIFO and Receive FIFO are user configurable from 128 to 2048 bytes each.



A block diagram of the SSN8006 is shown below.



The core is delivered as a synthesizable RTL Verilog model. Deliverables include:

- RTL Verilog source code model of the core
- Verilog testbench and test cases
- Synthesis scripts examples
- Complete detailed documentation and training class notes