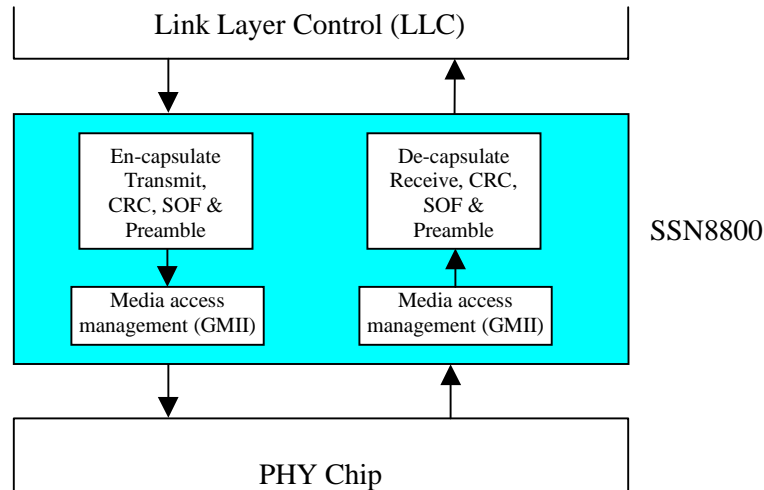




SSN8800: Ethernet 10/100/1000 MAC Core

The SSN8800 is an Ethernet 10/100/1000mb/s Media Access Controller. It adds Gigabit Ethernet (IEEE 802.3z) operation to the Ethernet 10/100 (IEEE 802.3) function to implement a complete Ethernet 10/100/1000 Triple Media Access Controller (MAC). A block representation of SSN8800 as per the IEEE standard specifications is shown below. The Ethernet 10/100/1000 MAC Core is available as a synthesizable Verilog model from Aurora VLSI, Inc. Contact CustomerService@auroravlsi.com.



Transmit data is transferred from the LLC to the SSN8800. The SSN8800 packages the data, including Preamble, SOF, PAD bytes as needed, and FCS. When the transmitter is not in the deferred mode, packets are transmitted to the PHY. The industry standard GMII (or TBI) interface is used to transfer the packet to the PHY chip. Upon each frame transmission, the transmit status is transferred back to the application.

Received data is checked for size and FCS correctness, and its destination address is filtered. Then if it passes address filtering, the received data is transferred to the LLC. If the length field in the frame is less than the minimum frame size, the PAD bytes are stripped from the frame. All of these operations can be enabled or disabled through the SSN8800 configuration registers. When a frame is received, its receive status is also transferred to the application.

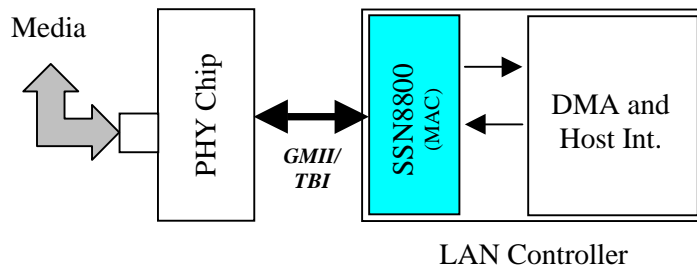
Features are summarized:

- Simple request/acknowledge interface to the application logic
- IEEE 802.3z compliant
- Full and half duplex
- Supports full duplex flow control (IEEE 802.3x)
- Automatic retries after collision, programmable retry counter
- Automatic padding and removal of the PAD bytes for minimum frame size
- FCS generation for transmit, and check for receive packets
- Supports carrier extension and packet bursting
- Industry standard MII, GMII, RGMII, and TBI interfaces to the PHY
- Includes PCS block for SERDES interface to optical Gigabit PHY
- MDIO interface for PHY management
- Programmable address filtering

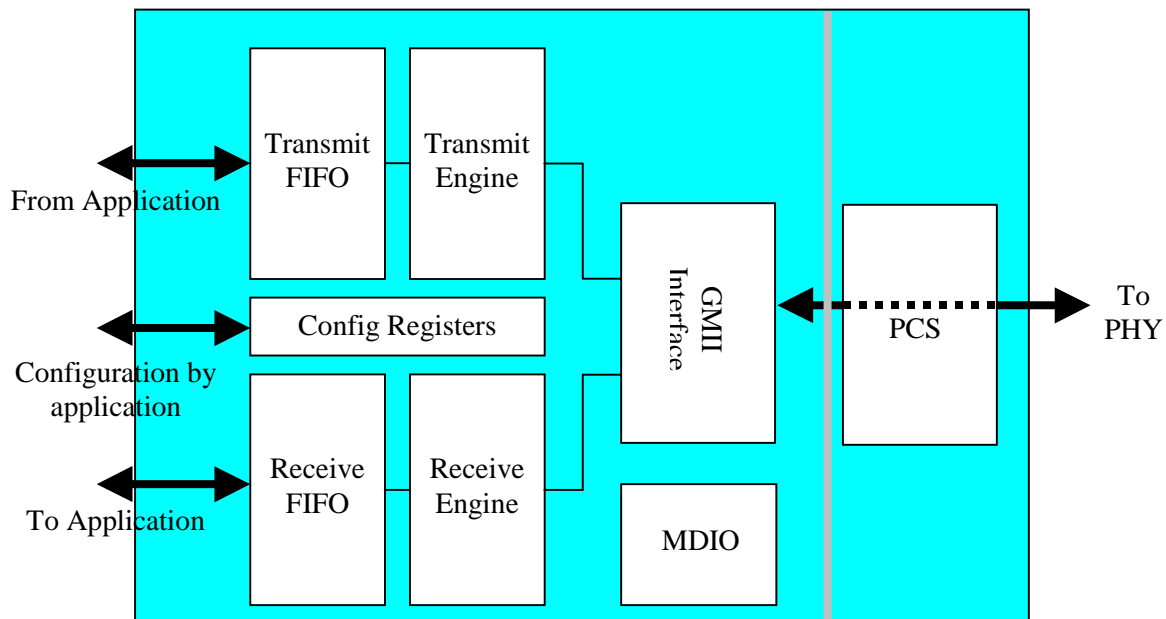


Use of the SSN8800 Ethernet 10/100/1000 Mac Core is shown below. The PHY interface is the industry standard Media Independent Interface- MII, Gigabit Media Independent Interface (GMII), Reduced Gigabit Media Independent Interface (RGMII), or Ten Bit Interface (TBI), as determined by a configuration register. Two versions of the Ethernet 10/100/1000 MAC Core are available. One version supports the TBI PHY interface, and the other version does not support it.

The interface between the application and the SSN8800 is a simple, easy to use FIFO interface. The sizes of the Transmit FIFO and Receive FIFO are user configurable from 512 to 8192 bytes each.



A block diagram of the SSN8800 is shown below.



The core is delivered as a synthesizable RTL Verilog model. Deliverables include:

- RTL Verilog source code model of the core
- Verilog testbench and test cases
- Synthesis scripts examples
- Complete detailed documentation and training class notes