



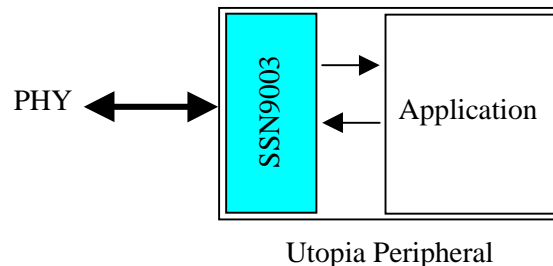
SSN9003: Utopia 1/2/2+/3/3+ Master Core

This core is an interface between UTOPIA/POS-PHY compliant PHY Chips and the application layers such as ATM. It operates in full duplex mode with PHY devices and supports up to 31 devices with a maximum data rate of 3.2 Gb/s. It is compliant to UTOPIA Level 3, Level 2, Level 1 Standards and POS-PHY Level 2 and 3 standards. Its mode can be switched between U1, U2 and U3. It is the Utopia master. The Utopia Core is available as a synthesizable Verilog model from Aurora VLSI, Inc. Contact CustomerService@auroravlsi.com.

Features are summarized:

- Supports both ATM Forum's standards and Saturn Group's POS-PHY Interface standards.
- Programmable option for U1, U2, U2+(or POS-PHY Level 2), U3, and U3+ standards.
- Supports both packet and cell level transfers.
- Number of ports for polling can be programmed.
- Receive Ports can be enabled or disabled dynamically.
- Transfer (PHY to core transfer length for every transfer) count can be independently programmed for each port with a maximum of 64 bytes.
- Round robin mechanism of polling on the receive side.
- Parity generation/checking with a programmable polarity option.
- User defined (through Verilog parameters) FIFO sizes for all transmit and receive FIFOs.
- Compatible receive and transmit application interfaces to design loop back at Utopia master level.
- Supports synchronous memories for FIFOs.
- Synthesis options for receive only, transmit only, or both receive and transmit.
- Simple configuration register interface to application logic.

The SSN9003 provides an application interface to which application logic can interface to the PHY. The application initiates transmit operations to the SSN9003 master. As the master, the SSN9003 polls ports to find receive data, and then brings the receive data into the SSN9003 Receive Data FIFO.



A block diagram of the SSN9003 is shown below.

The Utopia Core is a shell that holds a Receive Engine and Transmit Engine. The Receive Engine and Transmit Engine are completely independent of each other, with no interaction

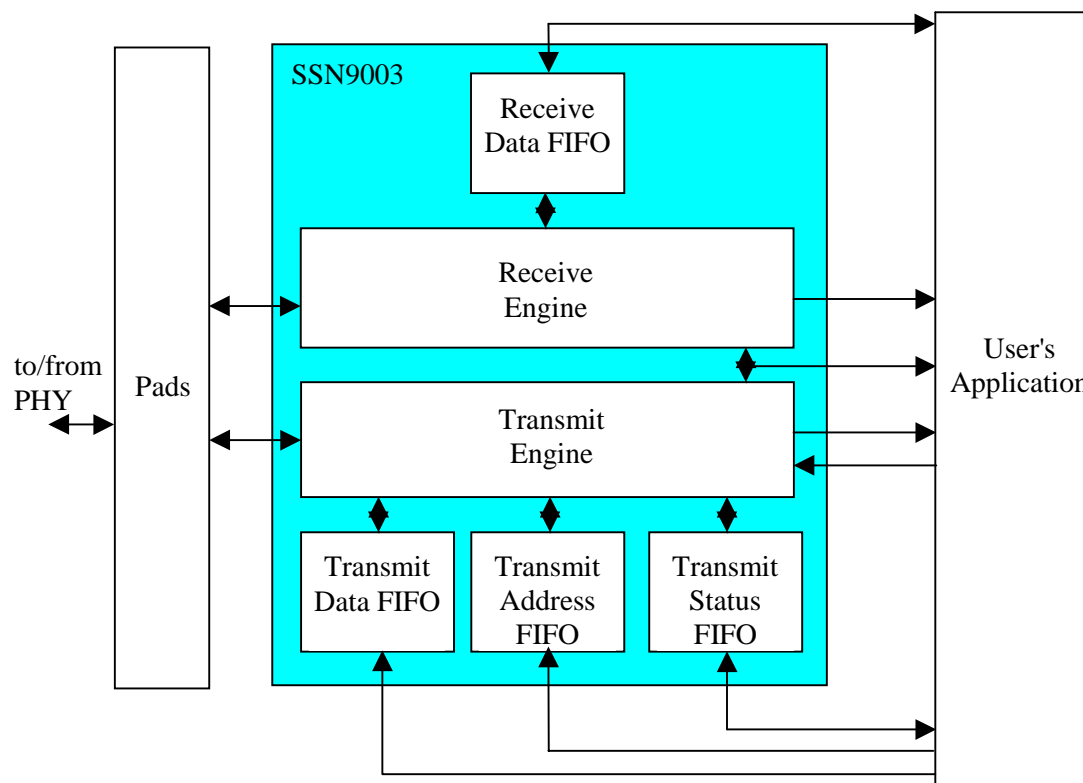


between them. The SSN9003 can be built with the Receive Engine and its FIFOs, or the Transmit Engine and its FIFOs, or both Receive and Transmit Engines and all FIFOs.

The Receive Engine receives data from the PHYs and provides it to the application logic. It includes Configuration Registers for receiving data.

The Transmit Engine transmits data to the PHYs from the application logic. It polls PHY ports to check if they are available to accept data transmitted to them in multi-PHY mode. (this is not necessary in single PHY mode), and provides this availability status to the application logic. It also includes Configuration Registers for transmitting data.

The FIFOs are non-synthesizable synchronous SRAM macros. The Receive Data FIFO holds incoming receive data from the PHY. The Transmit Address FIFO holds PHY port numbers to be polled to check if they are available to accept data transmitted from the SSN9003. The Transmit Status FIFO holds the status returned by each PHY when it is polled for its availability to accept data transmitted from the SSN9003. The Transmit Data FIFO holds outgoing transmit data for the PHY.



The core is delivered as a synthesizable RTL Verilog model. Deliverables include:

- RTL Verilog source code model of the core
- Verilog testbench and test cases
- Synthesis scripts examples
- Complete detailed documentation and training class notes