



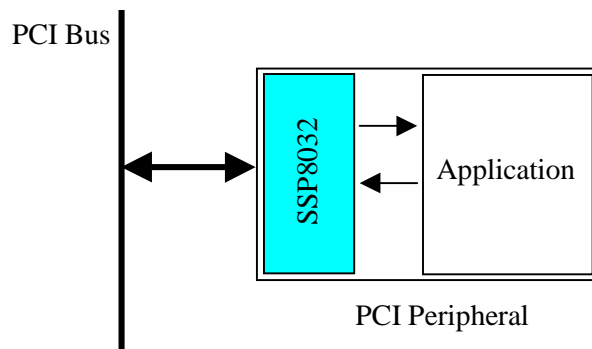
SSP8032: 32 Bit PCI Core

The SSP8032 PCI Core provides 32 bit PCI master and slave functionality. It is a 33/66MHz PCI core in ASIC technologies. It contains the standard PCI configuration registers including three base address registers. The 32 Bit PCI Core is available as a synthesizable Verilog model from Aurora VLSI, Inc. Contact CustomerService@auroravlsi.com.

Features are summarized:

- PCI 2.1 and 2.2 compliant
- Master and slave support 32 bit address and data transfers
- Supports variable burst size transfers
- Performs zero wait state transfers
- Master is capable of performing I/O, Memory and Configuration types of PCI transfers
- Master supports byte mode operation
- Master is capable of performing Memory Write Invalidate and Memory Read Line operations
- Performs back to back transfers
- Fully synchronous design

The SSP8032 provides a simple application interface to which any application logic can interface to the PCI bus. The application can initiate a PCI transaction through the SSP8032 in master mode. In slave mode, the PCI data is written to or read from the application.





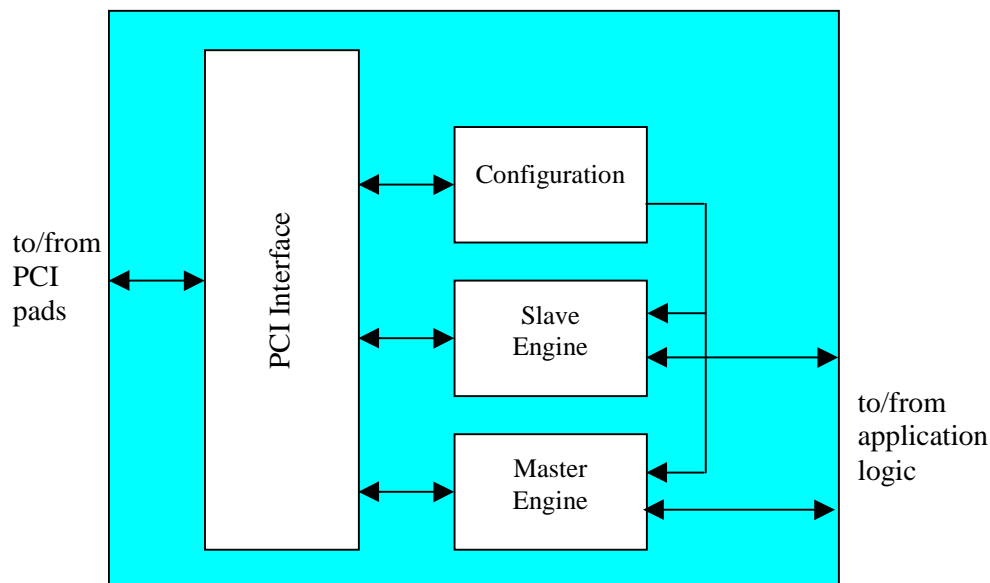
A block diagram of the SSP8032 is shown below.

The Master Engine handles master cycles, retries, command generation, and data transfers. It also handles Memory Write Invalidate (MWI) and Memory Read Line (MRL) transfers. It generates handshake signals to communicate with the application.

The Slave Engine handles address decode, command decode, and generation of slave PCI cycles. It is capable of performing burst transfers.

The Configuration block has the configuration address space of the SSP8032. It is programmable to accommodate multiple base address registers. It is addressed from both the application and the slave interface.

The PCI Interface communicates with the slave, configuration, and master data paths and address paths to generate appropriate transfers on the PCI bus. Pad control, data multiplexing, and parity generation and detection are performed in this block.



The core is delivered as a synthesizable RTL Verilog model. Deliverables include:

- RTL Verilog source code model of the core
- Verilog testbench and test cases
- Synthesis scripts examples
- Complete detailed documentation and training class notes