



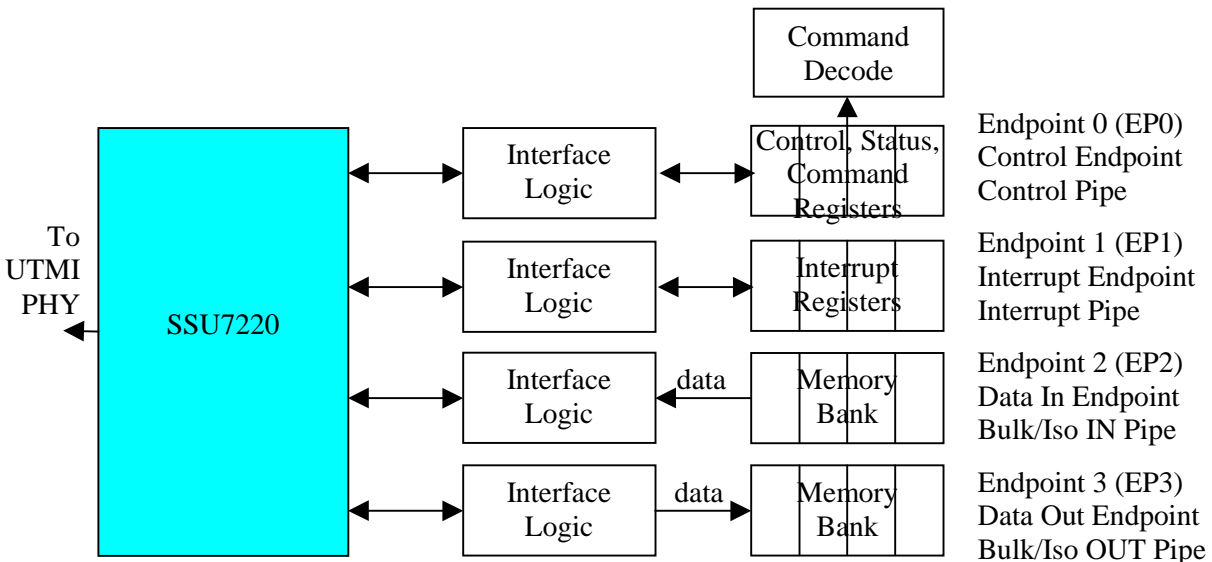
SSU7220: USB 2.0 Device Core (Mini Version)

The SSU7220 USB 2.0 Device Core provides USB 2.0 Device functionality. It minimizes gate count by including only the required endpoints plus two bulk/iso transfer endpoints. This USB 2.0 Device Core is available as a synthesizable Verilog model from Aurora VLSI, Inc. Contact CustomerService@auroravlsi.com.

Features are summarized:

- Four endpoints:
 - EP0- control endpoint, accepts SETUP, IN, and OUT control transactions
 - EP1- interrupt endpoint, accepts IN and OUT interrupt transactions
 - EP2- IN endpoint; accepts IN bulk and isochronous transactions
 - EP3- OUT endpoint; accepts OUT bulk and isochronous transactions
- 8 or 16 bit UTMI interface
- Accepts stalls from the application logic
- Low gate count

The application uses the two bulk/iso pipes for data transfer. Endpoint 2 (EP2) sends data over the bulk/iso IN pipe. Endpoint 3 (EP3) receives data from the bulk/iso OUT pipe. Data typically resides in SRAM memory banks at the two bulk/iso endpoints. The interrupt pipe is used for event notification- interrupts for events such as media change, media no longer ready, etc. The application posts interrupts in the Interrupt Registers, and the USB Host reads the interrupt registers with IN transactions to EP1. All the USB, class specific, and vendor specific commands are decoded and executed as register transfers through Control Endpoint- EP0. Configuration, interface, endpoint status registers, etc. are also accessed through EP0.



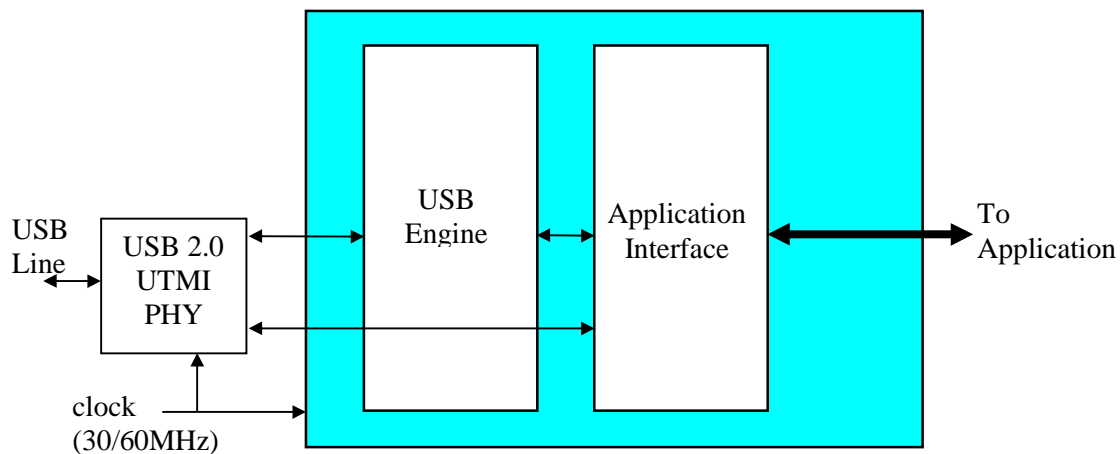


A block diagram of the SSU7220 is shown below.

There are two major blocks in SSU7220, the USB Engine and the Application Interface.

The USB Engine keeps track of a transaction on TXVALID, from SOP to EOP. On SOP, it checks the validity of the address and endpoint, and initiates the appropriate data transaction based on the status of the endpoint FIFOs. It handles the data retry mechanism using data toggling and generates appropriate handshakes.

The Application Interface provides a simple mechanism to interface to the user's logic. All endpoint FIFOs, registers, and any other memory elements are in the application logic. This interface allows direct access to all these endpoint FIFOs, registers, and other memory elements. It controls the addressing and control signals for the SSU7220 side of these memory elements. Setting and clearing of stall conditions are controlled by the application logic through the Application Interface. EP0, EP1, EP2, and EP3 endpoints are controlled independently. This allows simultaneous access to these endpoints.



The core is delivered as a synthesizable RTL Verilog model. Deliverables include:

- RTL Verilog source code model of the core
- Verilog testbench and test cases
- Synthesis scripts examples
- Complete detailed documentation and training class notes