



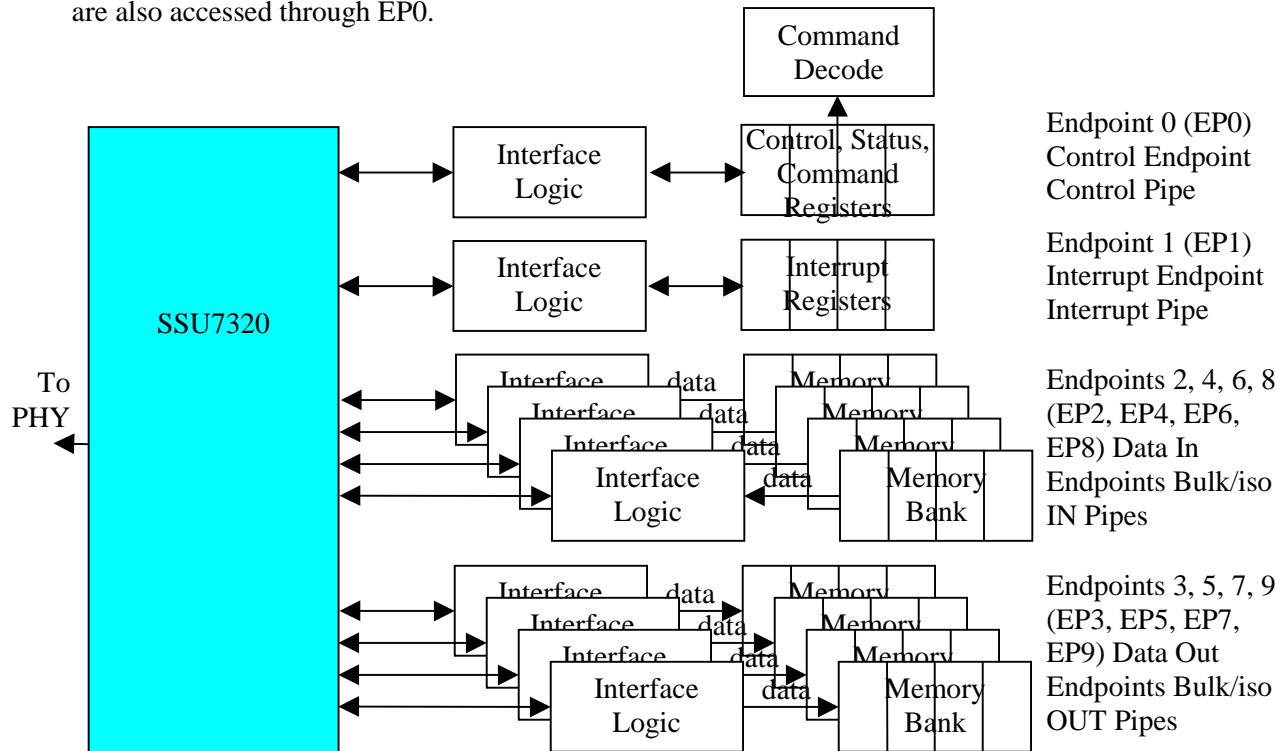
SSU7320: USB 2.0 Device Core

The SSU7320 USB 2.0 Device Core provides USB 2.0 Device functionality. It includes the required endpoints plus eight bulk/iso transfer endpoints. This USB 2.0 Device Core is available as a synthesizable Verilog model from Aurora VLSI, Inc. Contact CustomerService@auroravlsi.com.

Features are summarized:

- Ten endpoints:
 - EP0- control endpoint, accepts SETUP, IN, and OUT control transactions
 - EP1- interrupt endpoint, accepts IN and OUT interrupt transactions
 - EP2, EP4, EP6, EP8- IN endpoints; accept IN bulk and isochronous transactions
 - EP3, EP5, EP7, EP9- OUT endpoints; accept OUT bulk and isochronous transactions
- 8 or 16 bit UTMI interface
- Accepts stalls from the application logic

The application uses the eight bulk/iso pipes for data transfer. Endpoints 2, 4, 6, and 8 (EP2, EP4, EP6, and EP8) send data over bulk/iso IN pipes. Endpoints 3, 5, 7, and 9 (EP3, EP5, EP7, and EP9) receive data from bulk/iso OUT pipes. Data typically resides in SRAM memory banks at the bulk/iso endpoints. The interrupt pipe is used for event notification- interrupts for events such as media change, media no longer ready, etc. The application posts interrupts in the Interrupt Registers, and the USB Host reads the interrupt registers with IN transactions to EP1. All the USB, class specific, and vendor specific commands are decoded and executed as register transfers through Control Endpoint- EP0. Configuration, interface, endpoint status registers, etc. are also accessed through EP0.



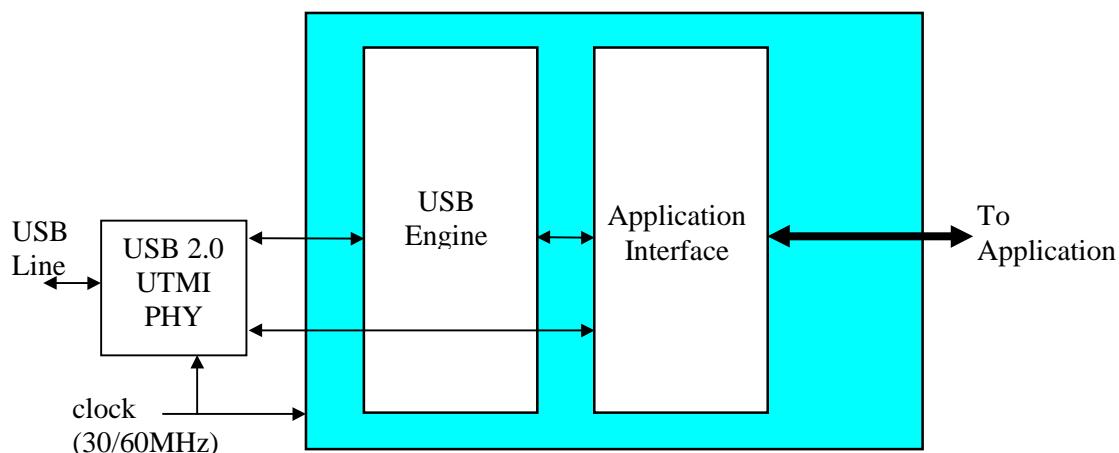


A block diagram of the SSU7320 is shown below.

There are two major blocks in SSU7320, the USB Engine and the Application Interface.

The USB Engine keeps track of a transaction on TXVALID, from SOP to EOP. On SOP, it checks the validity of the address and endpoint, and initiates the appropriate data transaction based on the status of the endpoint FIFOs. It handles the data retry mechanism using data toggling and generates appropriate handshakes.

The Application Interface provides a simple mechanism to interface to the user's logic. All endpoint FIFOs, registers, and any other memory elements are in the application logic. This interface allows direct access to all these endpoint FIFOs, registers, and other memory elements. It controls the addressing and control signals for the SSU7320 side of these memory elements. Setting and clearing of stall conditions are controlled by the application logic through the Application Interface. Each endpoint is controlled independently. This allows simultaneous access to any number of endpoints.



The core is delivered as a synthesizable RTL Verilog model. Deliverables include:

- RTL Verilog source code model of the core
- Verilog testbench and test cases
- Synthesis scripts examples
- Complete detailed documentation and training class notes